

| L<br>Number | Hits   | Search Text  | DB  | Time stamp          |
|-------------|--------|--|---|---------------------|
| 1           | 385588 | (primary or second\$6 or backup or back-up or (back adj1 up) or standby or redundan\$4 or spare\$4) same (processor or cpu or controller )   | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM_TDB | 2004/05/26<br>16:57 |
| 2           | 2091   | ((primary or second\$6 or backup or back-up or (back adj1 up) or standby or redundan\$4 or spare\$4) same (processor or cpu or controller ) ) same router  | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM_TDB | 2004/05/26<br>16:33 |
| 3           | 37     | ((primary or second\$6 or backup or back-up or (back adj1 up) or standby or redundan\$4 or spare\$4) same (processor or cpu or controller ) ) same router) same (switch\$6 adj1 fabric)  | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM_TDB | 2004/05/26<br>16:59 |
| 4           | 7      | (fail\$6 or fault\$6 or problem or error\$4 or malfunction) same (((primary or second\$6 or backup or back-up or (back adj1 up) or standby or redundan\$4 or spare\$4) same (processor or cpu or controller ) ) same router) same (switch\$6 adj1 fabric))   | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM_TDB | 2004/05/26<br>16:45 |
| 5           | 35     | (fail\$6 or fault\$6 or problem or error\$4 or malfunction) and (((primary or second\$6 or backup or back-up or (back adj1 up) or standby or redundan\$4 or spare\$4) same (processor or cpu or controller ) ) same router) same (switch\$6 adj1 fabric))  | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM_TDB | 2004/05/26<br>16:45 |
| 6           | 28     | ((fail\$6 or fault\$6 or problem or error\$4 or malfunction) and (((primary or second\$6 or backup or back-up or (back adj1 up) or standby or redundan\$4 or spare\$4) same (processor or cpu or controller ) ) same router) same (switch\$6 adj1 fabric))) not ((fail\$6 or fault\$6 or problem or error\$4 or malfunction) same (((primary or second\$6 or backup or back-up or (back adj1 up) or standby or redundan\$4 or spare\$4) same (processor or cpu or controller ) ) same router) same (switch\$6 adj1 fabric)))                                     | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM_TDB | 2004/05/26<br>16:45 |
| 7           | 26     | ((fail\$6 or fault\$6 or problem or error\$4 or malfunction) and (((primary or second\$6 or backup or back-up or (back adj1 up) or standby or redundan\$4 or spare\$4) same (processor or cpu or controller ) ) same router) same (switch\$6 adj1 fabric))) not ((fail\$6 or fault\$6 or problem or error\$4 or malfunction) same (((primary or second\$6 or backup or back-up or (back adj1 up) or standby or redundan\$4 or spare\$4) same (processor or cpu or controller ) ) same router) same (switch\$6 adj1 fabric))) and (7\$/\$.ccls. or 37\$/\$.ccls.) | USPAT;<br>US-PGPUB;<br>EPO; JPO;<br>DERWENT;<br>IBM_TDB | 2004/05/26<br>16:48 |

|          |              |   |  |                             |
|----------|--------------|---|--|-----------------------------|
| <b>8</b> | <b>42465</b> | <b>(primary or second\$6 or backup or back-up or (back adj1 up) or standby or redundan\$4 or spare\$4) adj2 (processor or cpu or controller )</b>   | <b>USPAT;<br/>US-PGPUB;<br/>EPO; JPO;<br/>DERWENT;<br/>IBM_TDB</b> | <b>2004/05/26<br/>16:58</b> |
| <b>9</b> | <b>3</b>     | <b>((primary or second\$6 or backup or back-up or (back adj1 up) or standby or redundan\$4 or spare\$4) adj2 (processor or cpu or controller ) ) same (switch\$6 adj1 fabric)<br/>same router</b> | <b>USPAT;<br/>US-PGPUB;<br/>EPO; JPO;<br/>DERWENT;<br/>IBM_TDB</b> | <b>2004/05/26<br/>16:59</b> |

DOCUMENT-IDENTIFIER: US 20030120991 A1

TITLE: Processor with packet data flushing feature

----- KWIC -----

Abstract Paragraph - ABTX (1):

A network processor or other type of processor includes first classification circuitry, scheduling circuitry and second classification circuitry. The first classification circuitry is configured to determine for a given packet received by the processor whether the packet has one or more errors. The scheduling circuitry in an illustrative embodiment receives an indication of the error determination made by the first classification circuitry, and based on the indication controls the dropping of the given packet from the processor memories if the packet has one or more errors, e.g., via a flush transmit command. The second classification circuitry, which may be implemented as a single classification engine or a set of such engines, may be configured to perform at least one classification operation for the given packet, e.g., if the packet is supplied thereto by the scheduling circuitry. Particular classification operations performed by at least one of the first and second classification circuitry are programmable via software that may be supplied to the processor via an associated host device. The processor may be configured as a network processor integrated circuit to provide an interface between a network and a switch fabric in a router or switch.

DOCUMENT-IDENTIFIER: US 20020144175 A1

TITLE: Apparatus and methods for fault-tolerant computing using a switching fabric

----- KWIC -----

Detail Description Paragraph - DETX (40):

[0056] In one embodiment of a fault-tolerant computer system 20, the system includes a first and second CPU nodes 151 and 151' (generally 151), one or more I/O nodes 170a, . . . 170n, 170m (generally 170), the switching fabric 150, and a first and second voting module 153, 153' (generally 153). Each of the end nodes 151, 170 is in communication with the switching fabric 150 through at least one communications link 160. The switching fabric 150 includes network components, such as switches, routers, repeaters, and transceivers interconnected through communications links 160. The communications links 160 may be serial communication links, parallel links, or broadband links. The communications links 160 may be implemented with "twisted-pair" cable, coaxial cable, fiberoptic cable, or wireless links, such as radio links or free-optics links.

US-PAT-NO: 6741552

DOCUMENT-IDENTIFIER: US 6741552 B1

TITLE: Fault-tolerant, highly-scalable cell switching architecture

----- KWIC -----

Detailed Description Paragraph Table - DETL (1):

TABLE 1 Glossary ABR Available Bit Rate ATM Asynchronous Transfer Mode  
CBR Constant Bit Rate CEC Cell Exchange Cycle of SCS Router CLP Cell Loss  
Priority field in ATM cell header EPD Early Packet Discard - packet discard  
mode where entire packet discarded in anticipation of buffer overflow egress  
referring to the SSE component that handles cells exiting the switch Gbps  
Gigabits Per Second GFC Generic Flow Control - field in ATM cell header HEC  
Header Error Correction - field in ATM cell header HOL Head of Line Blocking -  
Occurs in input buffered Blocking switches when a cell at head of input queue  
can't be accepted by switch because the required output resource is unavailable, but prevents a following cell whose output resource is available from moving through switch. hotspot a sink whose delivery capacity has been exceeded sink and deliverable cells are being retrograded ingress referring to the SSE component that handles cells input to the switch MIN Multi-Stage  
Interconnection Network IP Internet Protocol IPD Injection Packet Discard -  
packet discard mode at ingress SSE(s) initiated to alleviate congestion at egress SSE OAM referring to Operations and Maintenance cell - as indicated by a setting of the PTI field. Switch avoids discarding OAM cells, and may perform additional control processing on them. PCB Printed Circuit Board PCR  
Peak Cell Rate - cell transmission rate negotiated at call setup for ATM calls. Limits the burst rate of a call. PPD Partial Packet Discard - packet discard mode where remainder of packet discarded upon buffer overflow PBI  
Packet Boundary Indicator - a setting of PTI field to indicate the end of the packet. Switch avoids discarding a PBI cell. PTI Payload Type

Indicator - field in ATM cell header QoS Quality Of Service SCR Sustained Cell Rate - cell transmission rate negotiated at call set-up for ATM calls. Limits the aggregate bandwidth consumed by the call. SCS Saturated Constant Shuffle Routing Algorithm Algorithm for Hypercubes SCS Switch Fabric Element implementing SCS Algorithm Router SE Switching Element: a router (e.g., SCS Router), typically coupled with an SSE. sink destination port of call source input port of call SONET Synchronous Optical Network SSAC Source Sink ATM Controller - ATM specific SSE SSE Source Sink Element - provides ingress and egress port functions for hypercube generic cell switch UBR Unspecified Bit Rate VBR Variable Bit Rate VC Virtual Channel - shorthand for call switched on VC basis VCN Virtual Channel Number - internal switch call identifier, serves as index to VCR in VCR Table VCOP Virtual Channel Output Process - cell output process to manage access to output process VCQ VC Queue - per VC private queue space used for resequencing incoming cells and buffer output ready cells at egress port of switch VCR Virtual Channel Record - stores call state information at switch ports VCR Virtual Channel Record Table - table of call Table state information VLSI Very Large Scale Integration VP Virtual Path - a logical association or bundle of VCs VPI/VCI Virtual Path Identifier/ Virtual Channel Identifier - ATM cell header field identifying call

US-PAT-NO: 6078963

DOCUMENT-IDENTIFIER: US 6078963 A

TITLE: Router with de-centralized processing using  
intelligent ports

----- KWIC -----

Detailed Description Text - DETX (20):

Referring to FIG. 3, an intelligent router port 103 may maintain a routing table and/or a route cache table by first receiving a routing protocol packet (step 300) from another network node external to the router 100 via the external interface 201 and/or from another intelligent router port 103 within the router 100 via the internal interface 202. These interfaces 201, 202 may perform physical (OSI Layer 1) and/or data link (OSI Layer 2) layer processing of the routing protocol packet (step 305). The Layer 1 and 2 functions may include, for example, electrical circuit control, data bit transfer, data error detection, and/or data error recovery. After receiving and processing the routing protocol packet, the interfaces 201, 202 may transfer the routing protocol packet to the bus 205. The processor 200 may receive the routing protocol packet via the bus 205 and may update routing tables stored in the first level cache, second level cache, and/or routing table data storage 222 (step 310). The processor 200 may also broadcast a routing update to the other intelligent router ports 103, for instance across the switching fabric 102. The processor 200 may further forward a routing update to neighboring routers in the network using well-known protocols such as RIP, OSPF, and/or BGP4.